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EXAMINER	
BRINEY III, WALTER F	

ART UNIT	PAPER NUMBER
2644	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/605,953	FISCHER ET AL.	
	Examiner	Art Unit	
	Walter F Briney III	2644	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2, and 4-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, and 5 are rejected under 35 U.S.C. 102(e) as being anticipated by Murphy et al. (6,567,520).

Claim 1 is limited to **a circuit for detecting whether a telecommunication line is off-hook, said telecommunication line comprising tip and ring signal lines**. Murphy discloses **a voltage divider** (figure 3, elements R_i, R_1, R_2) **for coupling between said tip and ring lines and having a node** (figure 3, between R_i and R_1) **at which is presented a scaled version of a voltage across said voltage divider**. Murphy discloses a differential amplifier (i.e. **a transistor) having a control terminal coupled to said node** (figure 3, element 30, negative input) **and a first current flow terminal coupled to a voltage source** (figure 3, element 30, power references on bottom of amplifier) **and a second current flow terminal** (figure 3, element 30, output). Murphy discloses **an analog-to-digital converter** (figure 2, element 24) **having an analog input and a digital output, said analog input coupled to said second**

current flow terminal of said transistor (figure 2, element 22's output connected to element 24's input). Therefore, Murphy anticipates all limitations of the claim.

Claim 2 is limited to **the circuit of claim 1**, as covered by Murphy. Murphy discloses **a first resistor** (figure 3, element R_i) **having a first terminal for coupling to said tip line and a second terminal coupled to said node**. Murphy discloses **a second resistor** (figure 3, element R2) **having a first terminal for coupling to said ring line and a second terminal coupled to said node**. Therefore, Murphy anticipates all limitations of the claim.

Claim 5 is limited to **the circuit of claim 2**, as covered by Murphy. Murphy discloses **a processor coupled to said digital output of said analog-to-digital converter** (figure 2, element 26)**, said processor adapted to determine whether said telecommunication line is off-hook based on a signal on said digital output of said analog-to-digital converter** (column 2, lines 51-59). Therefore, Murphy anticipates all limitations of the claim.

Claims 27-32, 34, and 35 are rejected under 35 U.S.C. 102(b) as being anticipated by the applicant's admitted prior art.

Claim 27 is limited to **a method for detecting whether a telecommunication line is off-hook without affecting the line impedance, said telecommunication line comprising tip and ring signal lines, said method comprising the steps of: (1) modulating a DC voltage that appears across said tip and ring lines**; the admitted prior art discloses passing voltage between TIP and RING lines to a digital domain using voltage division, comparison, and isolation (i.e. modulating) (figure 1, PC Power

Domain and page 3, lines 3-16). **(2) passing said modulated DC voltage through an electrical high voltage interface circuit**; the prior discloses comparator's output (i.e. modulated DC voltage) is passed through an optical coupler (i.e. high voltage interface) (figure 1, element 28). **(3) determining whether said telecommunication line is off-hook as a function of said modulated DC voltage**; the prior discloses using a DSP (figure 1, element 25 and page 4, lines 11-22) to determine hook-state based on the voltage comparator's output (i.e. modulated DC voltage). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 28 is limited to **the method of claim 27**, as covered by the admitted prior art, **wherein step (1) comprises converting said DC voltage appearing across said tip and ring lines from analog to digital**; the admitted prior art discloses converting the voltage divider output to one of two states (i.e. converting from analog to digital) using the comparator (page 4, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 29 is limited to **the method of claim 28**, as covered by the admitted prior art, **further comprising the step of: (4) scaling said analog DC voltage appearing across said tip and ring lines before step (1)**; the admitted prior art discloses voltage dividing the tip and ring lines (figure 1, element 17 and page 3, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 30 is rejected for the same reasons as claim 29.

Claim 31 is limited to **the method of claim 27**, as covered by the admitted prior art, **wherein step (3) comprises comparing said modulated DC voltage to a**

reference value; the voltage divided output (i.e. modulated DC value) is compared to a reference value (figure 1, element 26). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 32 is limited to **the method of claim 31**, as covered by the admitted prior art, **wherein step (3) is performed by a digital signal processor**; the admitted prior art discloses passing the digital output to a digital signal processor that further determines the hook state (page 4, lines 11-22). Therefore, the admitted prior art makes obvious all limitations of the claim.

Claim 34 is limited to **the method of claim 29**, as covered by the admitted prior art, **further comprising the steps of (6) converting said DC voltage to a two state signal indicative of said DC voltage before step (1)**; the admitted prior art discloses converting the voltage divider output to a two-state signal based on its voltage using a comparator (page 4, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim 35 is limited to **the method of claim 34**, as covered by the admitted prior art, **wherein step (6) comprises controlling a transistor to turn on or off responsive to said DC voltage appearing across said tip and ring lines**. The admitted prior art discloses that a transistor that is part of an optical coupler (figure 1, element 28) turns on or off based on the output of a comparator (figure 1, element 24 and page 4, lines 3-11). Therefore, the admitted prior art discloses all limitations of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy.

Claim 4 is limited to **the circuit of claim 3**, as covered by Murphy. Murphy discloses a differential amplifier (figure 3, element 30), but does not disclose its reference power supply. Therefore, Murphy anticipates all limitations of the claim with the exception **wherein said voltage of said voltage source is ground**. The examiner takes Official Notice of the fact that using ground as a power supply is well-known. It would have been obvious to one of ordinary skill in the art at the time of the invention to reference the differential amplifier between ground and another value for the purpose of providing a current sink that is resilient to power fluctuations.

Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Scott et al. (US Patent 6,160,885).

Claim 6 is limited to **the circuit of claim 2**, as covered by Murphy. Murphy discloses **a differential converter** (figure 2, element 24) **comprising first and second analog input terminals** (figure 2, output from 22 and V_{ref}). Murphy discloses using the analog-to-digital converter for the purpose of detecting the hook-state of a telephone on a telephone line, but discloses no means to directly connect tip and ring signals to the analog-to-digital converter. Therefore, Murphy anticipates all limitations of the claim

with the exception of **said first analog input terminal coupled to said tip line and said second analog input terminal coupled to ring**. Scott teaches that an analog-to-digital converter used for hook-state detection can be multiplexed between the former function and caller-id detection (figure 18, elements 1814, 1815, 1810, TIP, RING) (column 27, line 58-column 28, line 12). By coupling tip and ring lines to the converter through a multiplexer, the converter can be reused, thus avoiding part duplication. It would have been obvious to one of ordinary skill in the art at the time of the invention to multiplex the analog-to-digital converter as taught by Scott for the purpose of reducing parts needed for hook-state and caller-id circuits.

Claim 7 is limited to **the circuit of claim 6**, as covered by Murphy in view of Scott. Scott teaches multiplexing an analog-to-digital converter between caller-id and hook-state circuitry. When caller-id signals are multiplexed to the analog-to-digital converter the input comprises **a first capacitor coupled between said tip line and said first analog input terminal of said analog-to-digital converter and a second capacitor coupled between said ring line and second analog input terminal of said analog-to-digital converter** (figure 18, elements 1703). Therefore, Murphy in view of Scott makes obvious all limitations of the claim.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of Scott and further in view of Yong et al. (US Patent 5,255,094).

Claim 8 is limited to **the apparatus of claim 7**, as covered by the Murphy in view of Scott. Murphy in view of Scott has been shown to disclose all limitations of the claim with the exception of **a diode having an anode coupled to said node and a cathode**

coupled to a control signal; Yong teaches to couple the anode of a diode to an amplifier (i.e. differential amplifier of Murphy) and a cathode to a transient protection circuit (i.e. control signal) (figure 2, element 42) for the purpose of providing a shunt for transients when power is first applied to a circuit (column 3, lines 28-40). It would have been obvious to one of ordinary skill in the art at the time of the invention to apply the transient protection circuit of Yong to the input of the comparator of Murphy for the purpose of protecting the input of the comparator to transients when power is suddenly applied to the comparator. **Said control signal having a first state which turns said diode on and drives said node to a voltage that turns said transistor off**; Yong teaches a power supply that is turned off (i.e. first state) causing the diode to turn on, where the voltage present at the input to the comparator (i.e. node) will be shunted so the comparator's output will be low causing the transistor in the optical coupler to turn off (column 3, line 41 through column 4, line 5). **A second state that turns said diode off whereby said node is driven to a voltage dictate by said voltage across said tip and ring lines**; Yong teaches a power supply that turns on (i.e. second state) that turns the diode off, where the voltage present at the input is determined by the voltage divider across it, whose voltage is determined by the TIP and RING lines (column 3, line 41 through column 4, line 5). Therefore, Murphy in view of Scott and further in view of Yong makes obvious all limitations of the claim.

Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of the applicant's admitted prior art.

Claim 9 is essentially the same as claim 5, as covered by Murphy, with the additional limitation **wherein said processor is adapted to disable said first circuit responsive to said analog-to-digital converter receiving said second voltage and enable said first circuit responsive to said analog-to-digital converter receiving said first voltage**. Murphy discloses monitoring the hook status of POTS devices because certain devices connected to the line may need to recognize when POTS devices go off-hook. Therefore, Murphy discloses all limitations of the claim with the exception **wherein said processor is adapted to disable said first circuit**. The applicant's admitted prior art teaches detecting POTS device's state so only household device may use the line at any given time (page 1, line 10-page 2, line 19) (page 4, lines 3-14). Because the admitted prior art discloses using the DSP detector to disable the ability of a device to go off-hook, it is inherent that a **first circuit** exists to take a device off-hook. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the hook-state detector of Murphy for detecting the hook-state of POTS devices as taught by the applicant's admitted prior art for the purpose of allowing only one POTS device to access a telephone line at a time.

Claim 10 is rejected for the same reasons as in claim 2.

Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of the applicant's admitted prior art and further in view of Scott.

Claim 11 is limited to the apparatus of claim 10, as covered by Murphy in view of the applicant's admitted prior art. Murphy discloses **a differential converter** (figure 2, element 24) **comprising first and second analog input terminals** (figure 2, output

from 22 and V_{ref}). Murphy discloses using the analog-to-digital converter for the purpose of detecting the hook-state of a telephone on a telephone line, but discloses no means to directly connect tip and ring signals to the analog-to-digital converter. Therefore, Murphy anticipates all limitations of the claim with the exception of **said first analog input terminal coupled to said tip line and said second analog input terminal coupled to ring**. Scott teaches that an analog-to-digital converter used for hook-state detection can be multiplexed between the former function and caller-id detection (figure 18, elements 1814, 1815, 1810, TIP, RING) (column 27, line 58-column 28, line 12). By coupling tip and ring lines to the converter through a multiplexer, the converter can be reused, thus avoiding part duplication. It would have been obvious to one of ordinary skill in the art at the time of the invention to multiplex the analog-to-digital converter as taught by Scott for the purpose of reducing parts needed for hook-state and caller-id circuits.

Claim 12 is limited to **the circuit of claim 11**, as covered by Murphy in view of the applicant's admitted prior art and further in view of Scott. Scott teaches multiplexing an analog-to-digital converter between caller-id and hook-state circuitry. When caller-id signals are multiplexed to the analog-to-digital converter the input comprises **a first capacitor coupled between said tip line and said first analog input terminal of said analog-to-digital converter and a second capacitor coupled between said ring line and second analog input terminal of said analog-to-digital converter** (figure 18, elements 1703). Therefore, Murphy in view the applicant's admitted prior art and further in view of Scott makes obvious all limitations of the claim.

Claims 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy in view of the applicant's admitted prior art in view of Scott and further in view of Yong.

Claim 13 is limited to the apparatus of claim 12, as covered by Murphy in view of the applicant's admitted prior art and further in view of Yong. For the same reasons as in claim 8, it would have been obvious to use the diode as taught by Yong in the combination of Murphy and Scott.

Claim 14 is limited to **the apparatus of claim 13**, as covered by Murphy in view of the applicant's admitted prior art in view of Scott and further in view of Yong, **wherein said control signal is normally in said first state and is switched to said second state just before said first circuit is to take said apparatus off-hook**; Yong teaches that the diode is on (i.e. in first state) when power is newly applied and switched off (i.e. in second state) before and after a transient (i.e. before off-hook) (column 3, line 41 through column 4, line 5). Therefore, the Murphy in view of Scott and further in view of Yong makes obvious all limitations of the claim.

Claim 15 is rejected for the same reasons as in claim 14.

Claim 16 is limited to **the apparatus of claim 15**, as covered by Murphy in view of the applicant's admitted prior art in view of Scott and further in view of Yong. Murphy discloses a hook-state detector that requires the use of a digital-to-analog to amplifier to determine the polarity of a tip and ring line, however, handling polarity reversal can become complicated. Therefore, Murphy in view of Scott makes obvious all limitations of the claim with the exception of **a full wave rectifier circuit coupled between said**

detection circuit and said tip and ring lines. The examiner takes Official Notice of the fact that full-wave rectifier circuits coupled between tip and ring lines are well-known. It would have been obvious to one of ordinary skill in the art at the time of the invention to use a full-wave bridge rectifier between the tip and ring lines for the purpose of forcing one of the tip and ring lines to always be of a greater absolute value, therefore eliminating the need of the of complicated detection algorithm necessitated by Murphy.

Claim 17 is limited to **the apparatus of claim 15**, as covered by Murphy in view of the applicant's admitted prior art in view of Scott and in further view of Yong, **wherein said first and second inputs of said analog-to-digital converter are biased to common mode voltage**; Murphy discloses two inputs to the converter, the output of the voltage divider and a reference voltage. The voltage divider's output is derived form TIP and RING signals, which are biased to common mode voltage through the ground terminal via resistors R_1 and R_2. The reference voltage must be selected to account for this. Therefore, Murphy in view of Scott and in further view of Yong makes obvious all limitations of the claim.

Claim 18 is essentially the same as claim 4 and is rejected for the same reasons.

Claims 19-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Scott and in further view of Jamshidi (US Patent 5,646,558).

Claim 19 is limited to **a circuit for detecting whether a telecommunication line is off-hook, said telecommunication line comprising tip and ring signal lines**; the admitted prior art discloses a circuit for detecting hook status of tip and ring lines

(page 3, lines 3-7). **Said circuit comprising: a voltage divider for coupling between said tip and ring lines**; the admitted prior art discloses a voltage divider (figure 1, element 17) between tip and ring through lines tip' and ring', respectively. **Having first and second nodes across which appears a scaled version of a voltage across said tip and ring lines**; the admitted prior art discloses a node between two resistors (figure 1, element 22) and ground. **A differential analog-to-digital converter having first and second analog input terminals and a digital output terminal**; the admitted prior art discloses an analog-to-digital converter comprising a comparator (i.e. differential) and optical coupler (figure 1, elements 24 and 28) with an input from the first node and an input from ground (i.e. second node) with a bistable output. Therefore, the admitted prior art has been shown to disclose all limitations of the claim with the exception of **a signal line for selectively enabling said circuit when said signal is in a first state and disabling said circuit when said signal is in a second state; a first transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said first node and said first input terminal of said analog-to-digital converter; whereby, when said signal line is in said first state, said analog-to-digital converter receives a scaled version of the voltage across said tip and ring lines and, when said signal line is in said second state, said analog-to-digital converter receives no signal from said voltage divider**; Scott teaches to implement a multiplexer for the purpose of alternatively selecting between DC hook switch detection (i.e. voltage divider of the admitted prior art with first and second node) and AC tip and ring lines for the purpose of eliminating a

need for a separate caller-id interface (column 27, line 58-column 28, line 12). Therefore, it would have been obvious to implement a multiplexer at the input of the A/D converter of the admitted prior art as taught by Scott for the purpose of supplying means to connect tip and ring lines to the A/D converter thus eliminating the need for an extra hardware interface. Jamshidi teaches to build a multiplexer using pass gate logic that passes a transistor's input (i.e. first node) to its output (i.e. input of A/D) (i.e. enables analog-to-digital converter to receive a scaled version of the voltage across said tip and ring lines) when a control signal (i.e. signal line for selectively enabling) is in a first state and blocks the input of a transistor from reaching its output (i.e. disabling the analog-to-digital input from the voltage divider so no signal is received) when the control signal is in a second state (figure 7 and column 5, line 27 through column 6, lines 22) where the size of a single transistor pass gate saves on area (column 2, lines 5-15). It would have been obvious at the time of the invention to use pass gate multiplexers in the multiplexing arrangement of the admitted prior art in view of Scott for the purpose of saving area. **A second transistor having a control terminal coupled to said signal line and first and second current flow terminals coupled between said second node and said second input terminal of said analog-to-digital converter**; the admitted prior art teaches connecting two lines from the voltage divider to the input of the A/D (i.e. first node and second node), and using the pass-gate architecture of Jamshidi two transistors (i.e. first and second transistor) would inherently be needed for blocking and enabling both lines of the hook state detection circuitry. Therefore, the

admitted prior art in view of Scott and in further view of Jamshidi makes obvious all limitations of the claim.

Claim 20 is essentially the same as claim 2 and is rejected for the same reasons.

Claim 21 is limited to **the circuit of claim 20**, as covered by the admitted prior art in view of Scott and in further view of Jamshidi, **further comprising a diode coupled between said second node and said ring line**; the admitted prior art discloses a diode as part of a bridge rectifier between ground (i.e. second node) and RING via RING'. Therefore, the admitted prior art in view of Scott and in further view of Jamshidi makes obvious all limitations of the claim.

Claim 22 is essentially the same as claim 5 and is rejected for the same reasons.

Claim 23 contains the essence of claim 19 as covered by the admitted prior art in view of Scott and in further view of Jamshidi. Therefore, the admitted prior art in view of Scott and in further view of Jamshidi has been shown to make obvious all limitations of the claim with the exception of **a processor**; the admitted prior art discloses the use of a DSP (figure 1, element 25). **Said processor is adapted to disable said first circuit responsive to said analog-to-digital converter receiving said second voltage and enable said first circuit responsive to said analog-to-digital converter receiving said first voltage**; the admitted prior art discloses that the DSP (i.e. processor) (figure 1, element 25) is programmed to disable the telecommunication apparatus from going off-hook when the voltage across tip and ring is less than 30 volts (i.e. second voltage), but is enabled when the voltage is greater than 30 volts (i.e. second voltage) (page 4, lines 3-14). **A first circuit for taking said apparatus off-hook so that said**

apparatus may receive or transmit information via said telecommunication link; the admitted prior art discloses a DSP to disable the ability of the apparatus to go off-hook so inherently a circuit exists for taking the device off-hook to connect to a line (i.e. to transmit or receive). Therefore, the admitted prior art in view of Scott and in further view of Jamshidi makes obvious all limitations of the claim.

Claims 24-26 are essentially the same as claims 20-22, respectively, and are rejected for the same reasons.

Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art in view of Scott.

Claim 33 is limited to **the method of claim 29**, as covered by the admitted prior art, **further comprising the step of (5) selectively enabling said DC voltage appearing across said tip and ring lines to be modulated**. Scott teaches to implement a multiplexer for the purpose of selecting between hook switch detection and tip and ring lines (i.e. selectively enabling modulation) for the purpose of eliminating a need for a separate hardware interface (column 27, line 58 through column 28, line 12). Therefore, it would have been obvious to implement a multiplexer at the input of the A/D converter of the admitted prior art as taught by Scott for the purpose of supplying means to connect tip and ring lines to the A/D converter thus eliminating the need for an extra hardware interface.

Response to Arguments

Applicant's arguments with respect to claims 1-18 filed 23 January 2004 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments with respect to claims 19-35 filed 23 January 2004 have been fully considered but they are not persuasive.

With respect to claims 19-22, 23-26, and 33, **the applicant alleges that the comparator of the applicant's admitted prior art is not an analog-to-digital converter**; the examiner respectfully disagrees. It is clear that the comparator of the applicant's admitted prior art is an analog-to-digital converter because it has an analog input from the voltage divider and provides a digital output. The digital output is a single-bit representation of the analog input.

With respect to claims 19-22, 23-26, and 33, **the applicant alleges that the comparator (i.e. analog-to-digital converter) of the prior art is not useful in the A/D circuitry of Scott**; the examiner respectfully disagrees. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

With respect to claims 27-35, **the applicant alleges that the prior art does not disclose the electrical high-voltage barrier of claim 27 (page 19, fourth paragraph)**; the examiner respectfully disagrees. The prior art clearly includes an optical coupler (figure 1, element 28) that provides high-voltage isolation between two

electrical circuits. Hence, the optical coupler is an **electrical high-voltage interface circuit** as recited in claim 27.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter F Briney III whose telephone number is 703-305-0347. The examiner can normally be reached on M-F 8am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Forester W Isen can be reached on 703-305-4386. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

WFB
3/19/04

MINSUN OH HARVEY
PRIMARY EXAMINER